MULTIPLE GATE DIELECTRIC STRUCTURE AND METHOD FOR FORMING

Abstract of the Disclosure

Embodiments of the present invention relate to semiconductor structures having multiple gate dielectric structures. One embodiment forms semiconductor devices in multiple regions having different dielectric thicknesses where the interface between the gate dielectric and the semiconductor substrate is protected to result in an improved (e.g. less rough) interface. One embodiment includes forming a dielectric layer overlying a substrate, partially etching the dielectric layer in at least one of the multiple regions, and ashing the dielectric layer. The remaining portion of the dielectric layer (due to the partial etch) may then help protect the underlying substrate from damage during a subsequent preclean. Afterwards, in one embodiment, the gate dielectric layer is grown to achieve a target gate dielectric thickness in at least one of the regions. This may also help further densify the gate dielectric layer. Processing may then be continued to form semiconductor devices in each of the multiple regions.